FIG. 1

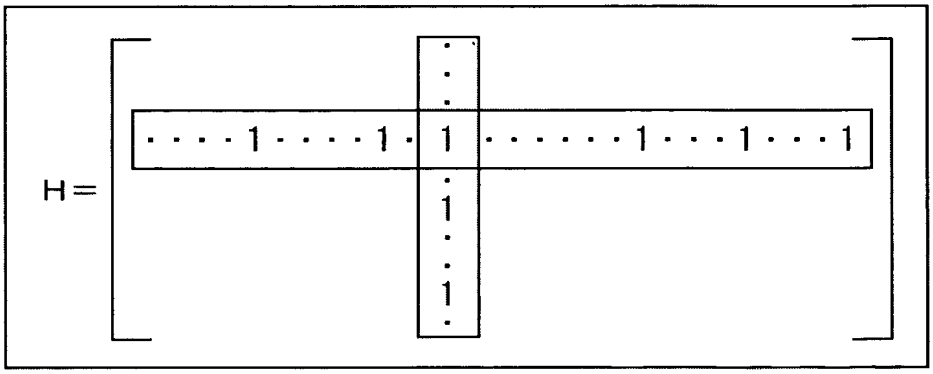


FIG. 2

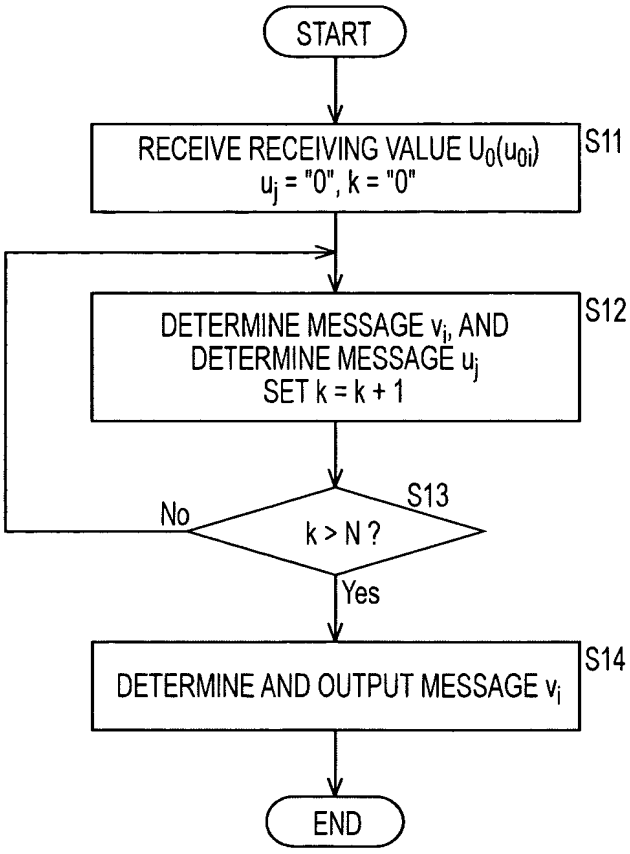

START
RECEIVE RECEIVING VALUE $U_0(u_{0i})$
u_j = "0", k = "0"
S11
DETERMINE MESSAGE v_i, AND
DETERMINE MESSAGE u_j
SET k = k + 1
S12
S13
No
k > N ?
Yes
DETERMINE AND OUTPUT MESSAGE v_i
S14
END

FIG. 3

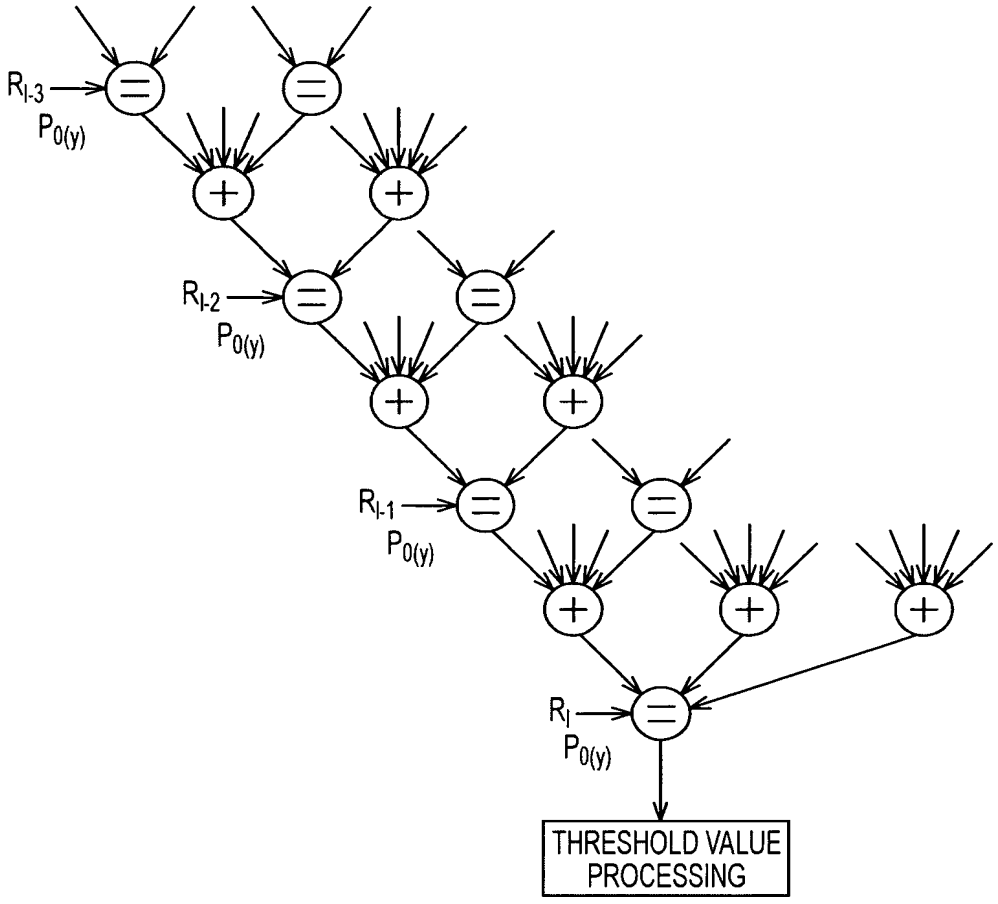


FIG. 4

$$H = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 1 & 1 \end{bmatrix}$$

FIG. 5

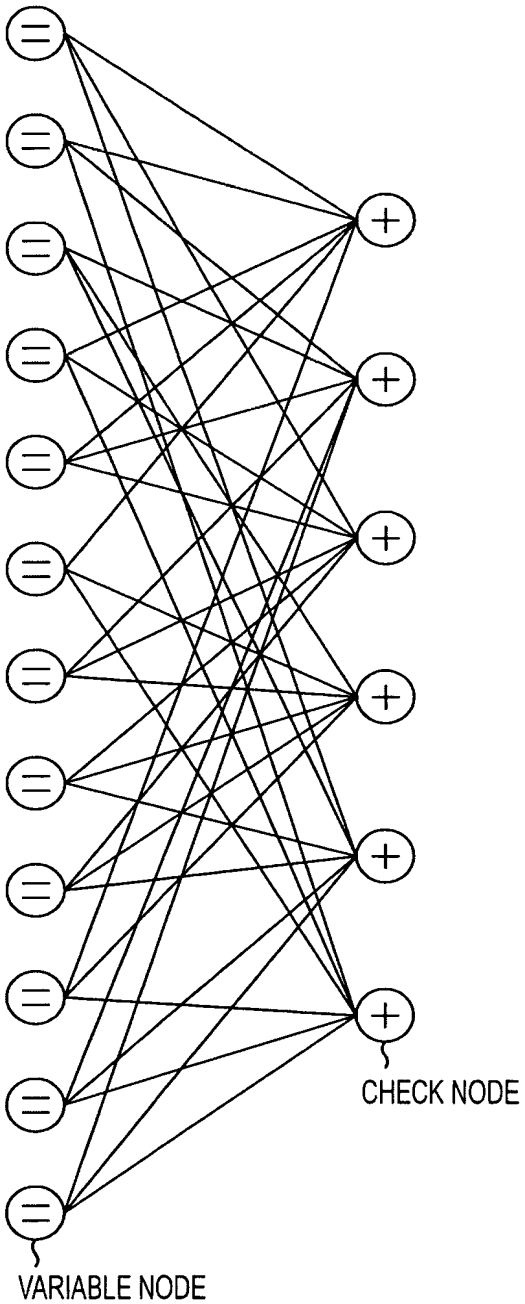


FIG. 6

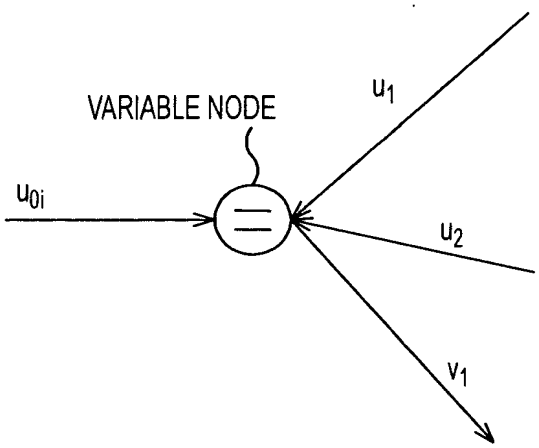


FIG. 7

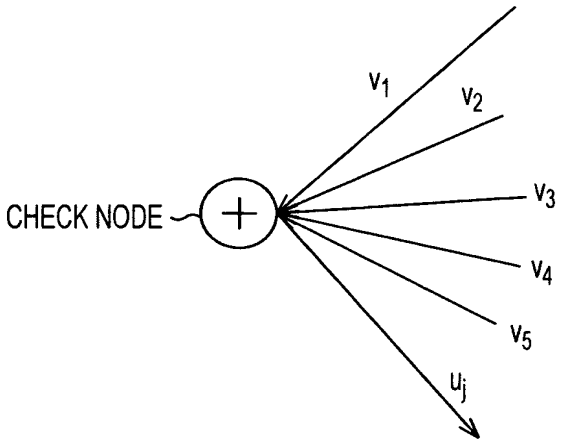


FIG. 8

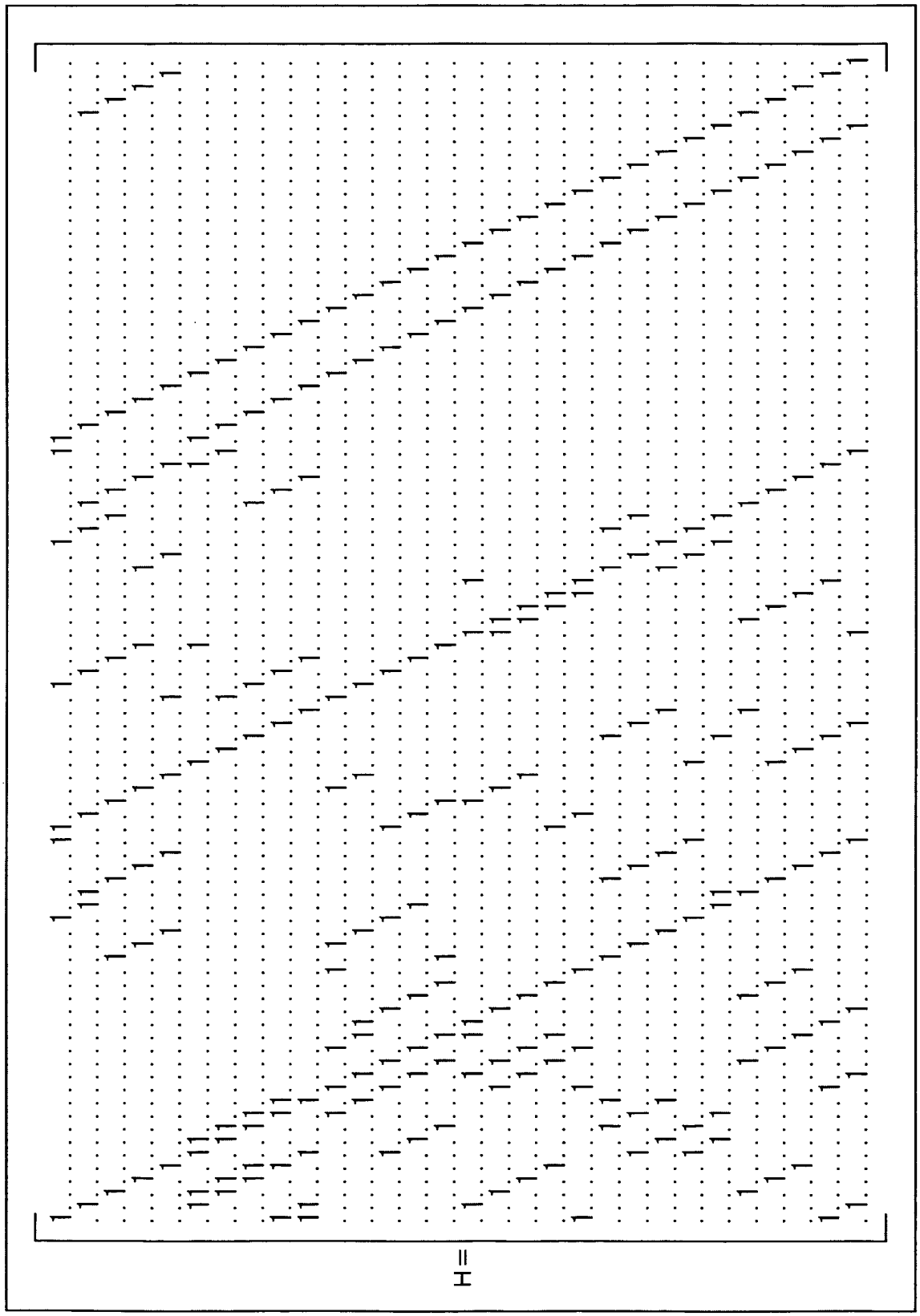


FIG. 9

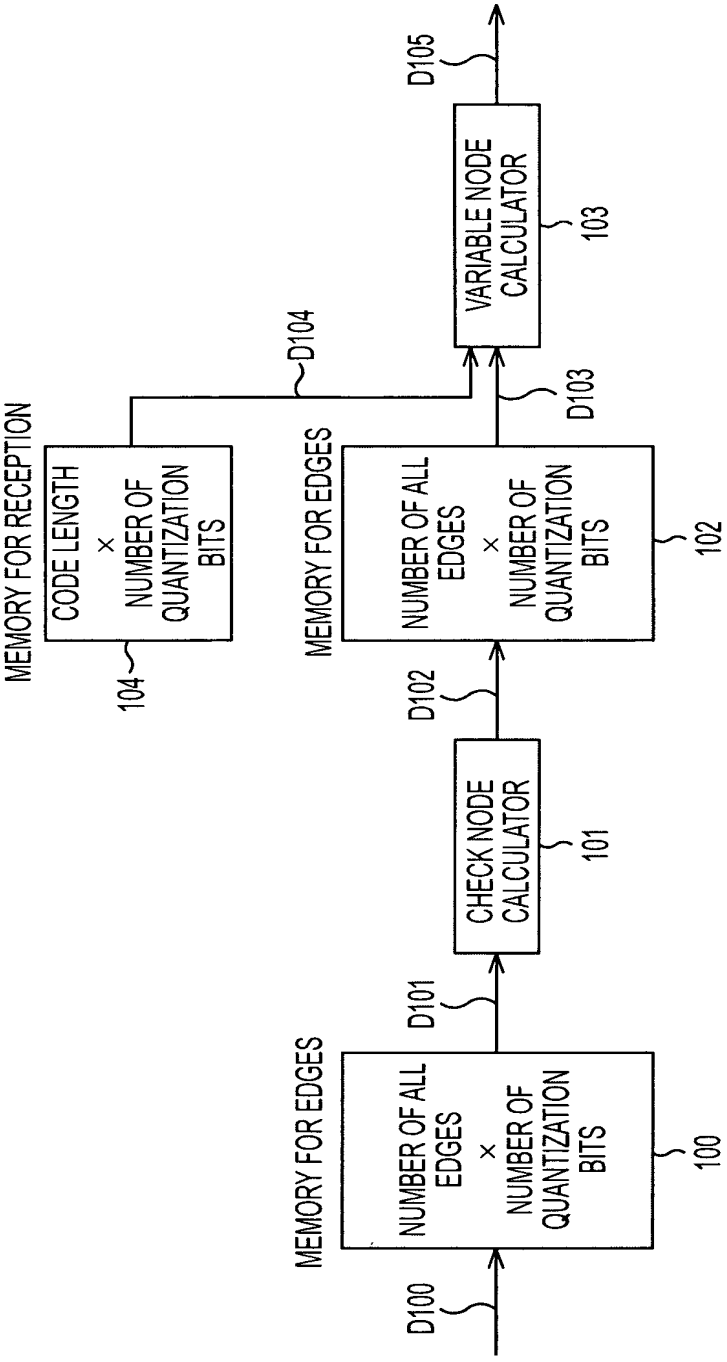

D100
MEMORY FOR EDGES
NUMBER OF ALL EDGES × NUMBER OF QUANTIZATION BITS
100
D101
CHECK NODE CALCULATOR
101
D102
MEMORY FOR EDGES
NUMBER OF ALL EDGES × NUMBER OF QUANTIZATION BITS
102
D103
VARIABLE NODE CALCULATOR
103
D105
D104
MEMORY FOR RECEPTION
CODE LENGTH × NUMBER OF QUANTIZATION BITS
104

FIG. 10

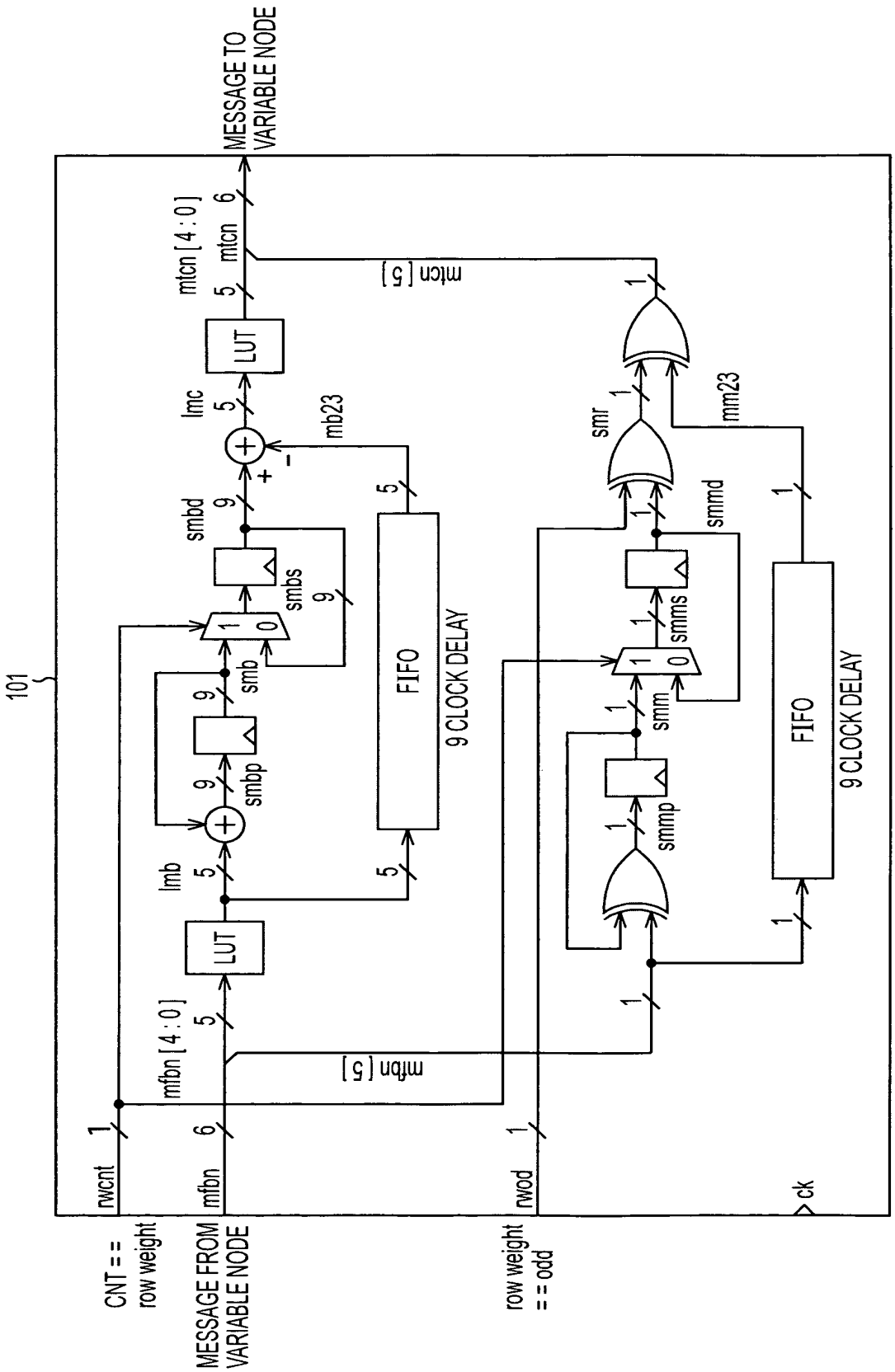

101
MESSAGE TO VARIABLE NODE
mtcn [4:0]
mtcn
LUT
lmc
mb23
smbd
smbs
smb
smbp
lmb
LUT
mfbn [4:0]
mfbn [5]
FIFO
9 CLOCK DELAY
smr
mm23
smmd
smms
smm
smmp
FIFO
9 CLOCK DELAY
nwcnt
mfbn
nwod
ck
CNT == row weight
MESSAGE FROM VARIABLE NODE
row weight == odd

FIG. 11

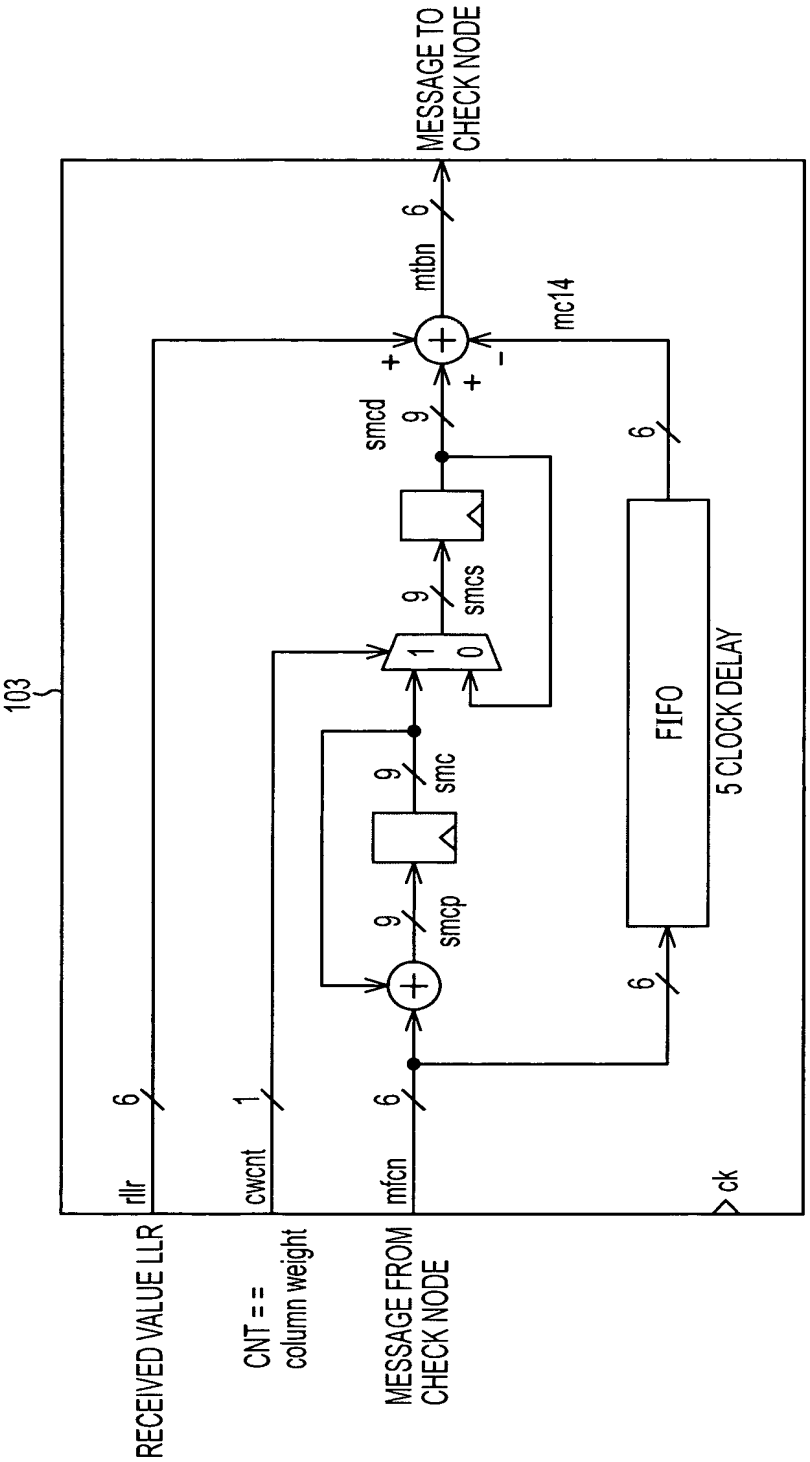

103
RECEIVED VALUE LLR
CNT = = column weight
MESSAGE FROM CHECK NODE
MESSAGE TO CHECK NODE
rllr
cwcnt
mfcn
ck
mtbn
mc14
smcd
smcs
smc
smcp
FIFO
5 CLOCK DELAY
6
1
9
0

FIG. 12A

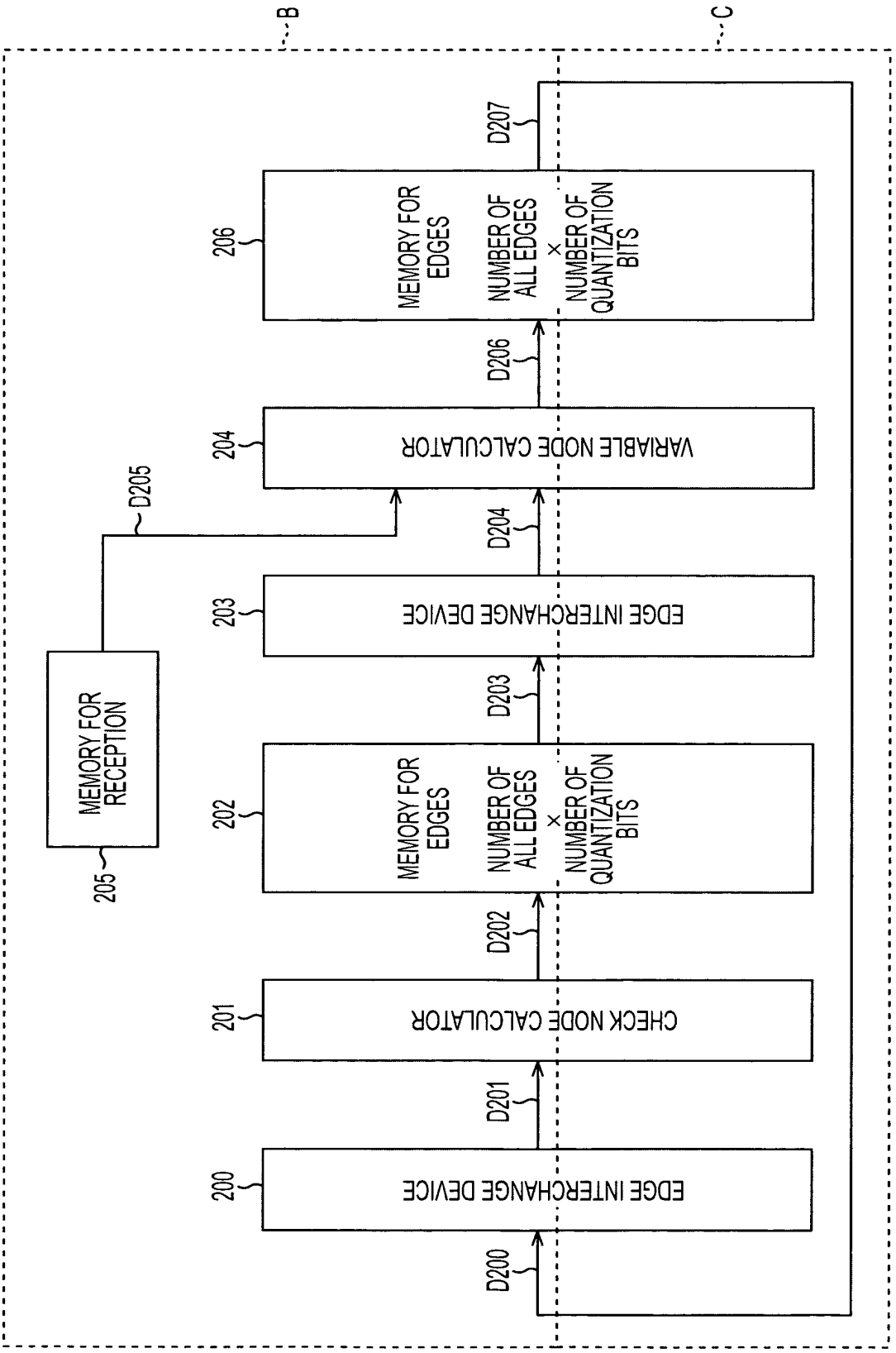

B
C
200
EDGE INTERCHANGE DEVICE
201
CHECK NODE CALCULATOR
202
MEMORY FOR EDGES
NUMBER OF ALL EDGES × NUMBER OF QUANTIZATION BITS
203
EDGE INTERCHANGE DEVICE
204
VARIABLE NODE CALCULATOR
205
MEMORY FOR RECEPTION
206
MEMORY FOR EDGES
NUMBER OF ALL EDGES × NUMBER OF QUANTIZATION BITS
D200
D201
D202
D203
D204
D205
D206
D207

FIG. 12B

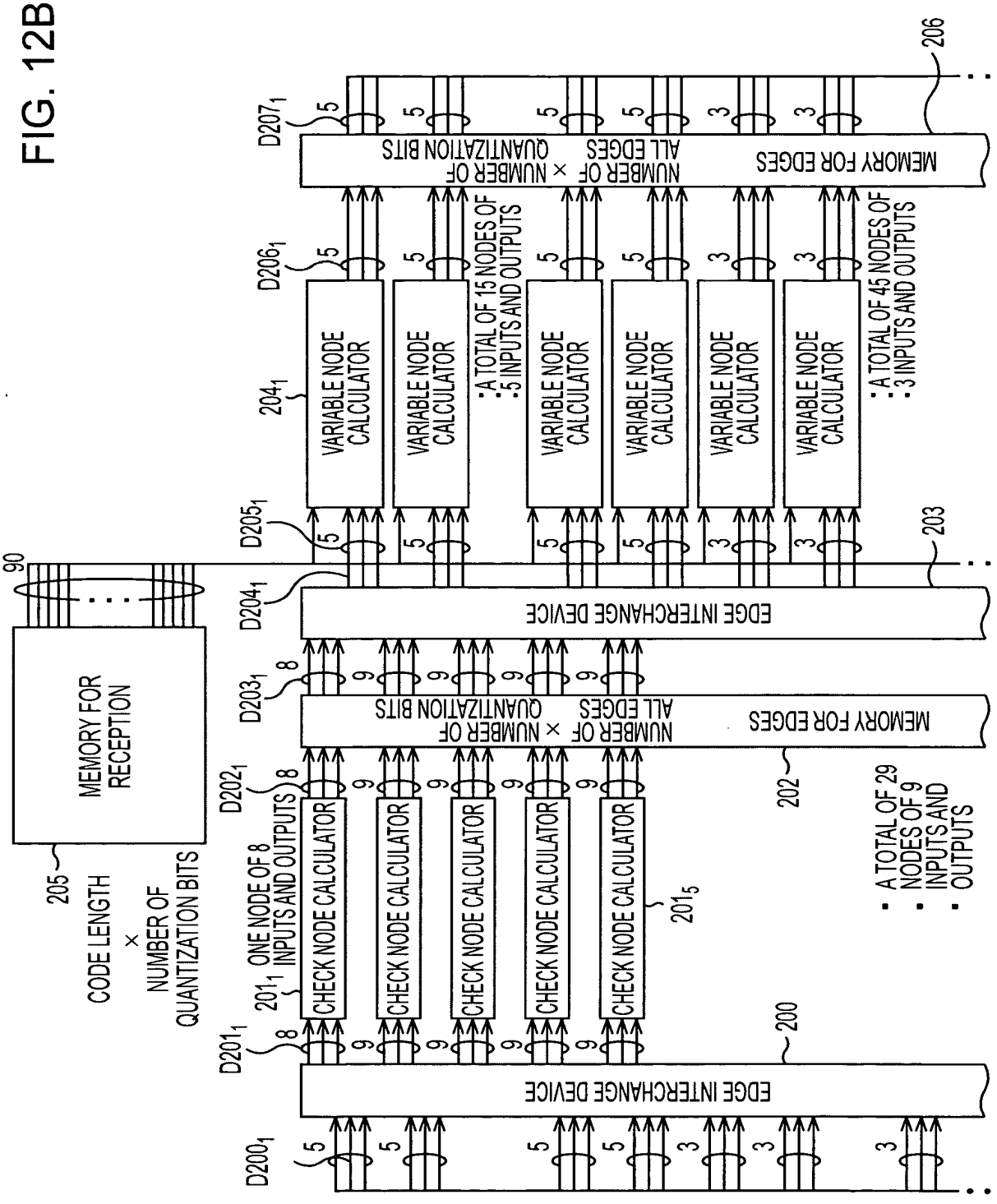

MEMORY FOR RECEPTION
CODE LENGTH × NUMBER OF QUANTIZATION BITS
205
90
EDGE INTERCHANGE DEVICE
MEMORY FOR EDGES
NUMBER OF ALL EDGES × NUMBER OF QUANTIZATION BITS
VARIABLE NODE CALCULATOR
CHECK NODE CALCULATOR
: A TOTAL OF 15 NODES OF : 5 INPUTS AND OUTPUTS
: A TOTAL OF 45 NODES OF : 3 INPUTS AND OUTPUTS
ONE NODE OF 8 INPUTS AND OUTPUTS
A TOTAL OF 29 NODES OF 9 INPUTS AND OUTPUTS
200
202
203
206

FIG. 12C

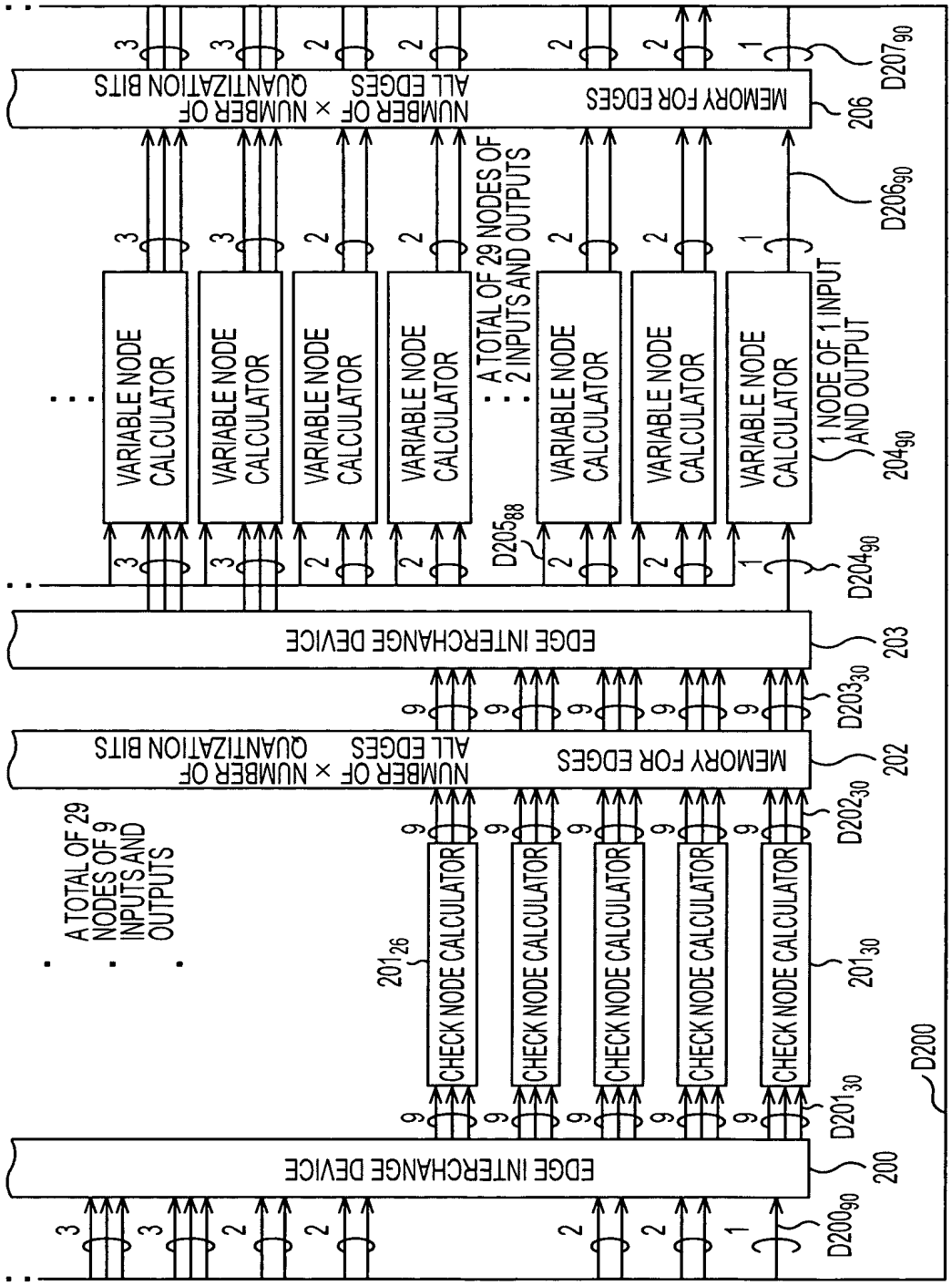

EDGE INTERCHANGE DEVICE
200
D200
D200$_{90}$
D201$_{30}$
CHECK NODE CALCULATOR
201$_{26}$
201$_{30}$
A TOTAL OF 29 NODES OF 9 INPUTS AND OUTPUTS
D202$_{30}$
MEMORY FOR EDGES
NUMBER OF ALL EDGES × NUMBER OF QUANTIZATION BITS
202
D203$_{30}$
EDGE INTERCHANGE DEVICE
203
D204$_{90}$
VARIABLE NODE CALCULATOR
204$_{90}$
1 NODE OF 1 INPUT AND OUTPUT
A TOTAL OF 29 NODES OF 2 INPUTS AND OUTPUTS
D205$_{88}$
D206$_{90}$
MEMORY FOR EDGES
NUMBER OF ALL EDGES × NUMBER OF QUANTIZATION BITS
206
D207$_{90}$

FIG. 13

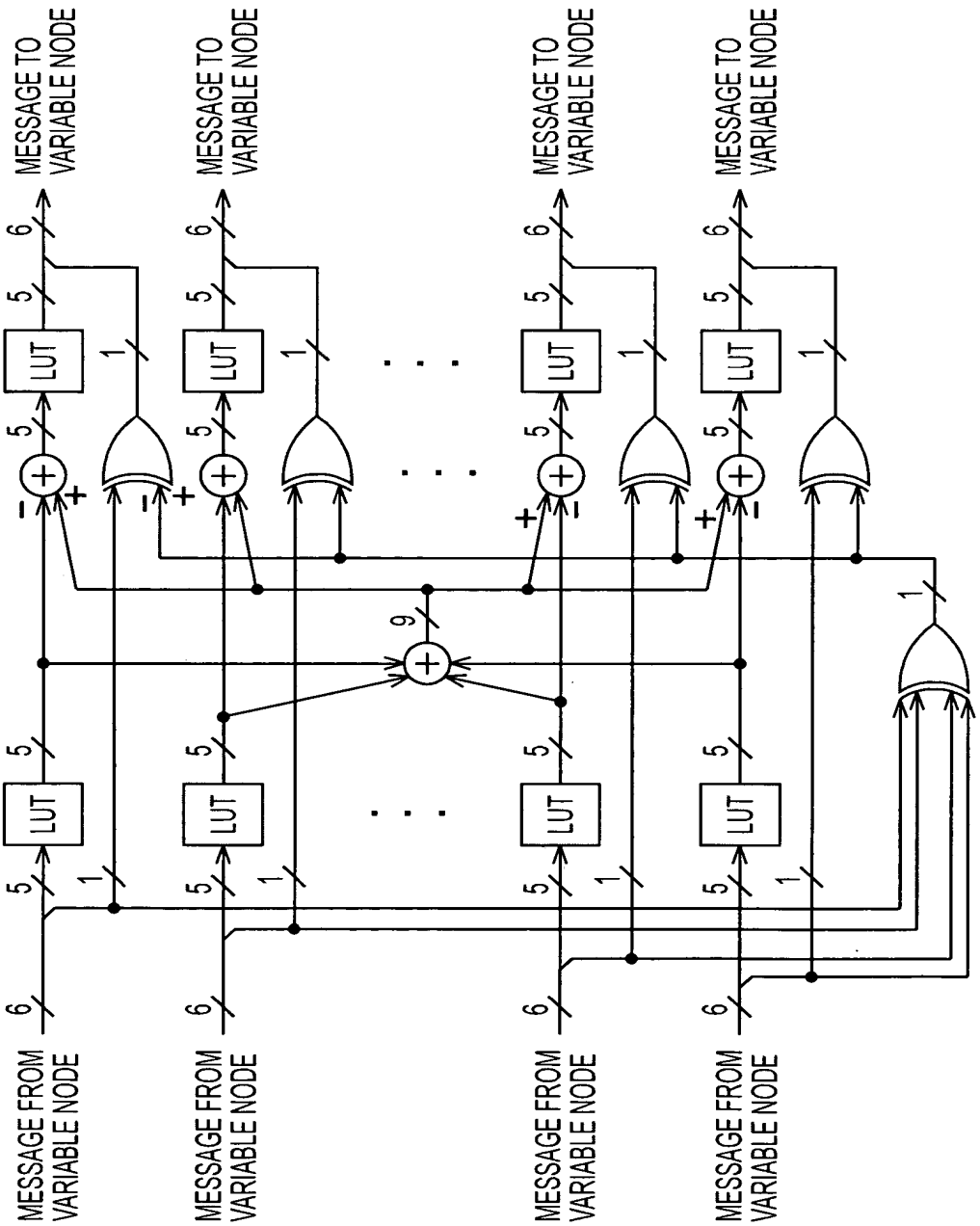

MESSAGE TO VARIABLE NODE
MESSAGE TO VARIABLE NODE
MESSAGE TO VARIABLE NODE
MESSAGE TO VARIABLE NODE
LUT
LUT
LUT
LUT
LUT
LUT
LUT
LUT
MESSAGE FROM VARIABLE NODE
MESSAGE FROM VARIABLE NODE
MESSAGE FROM VARIABLE NODE
MESSAGE FROM VARIABLE NODE
6
5
1
9

FIG. 14

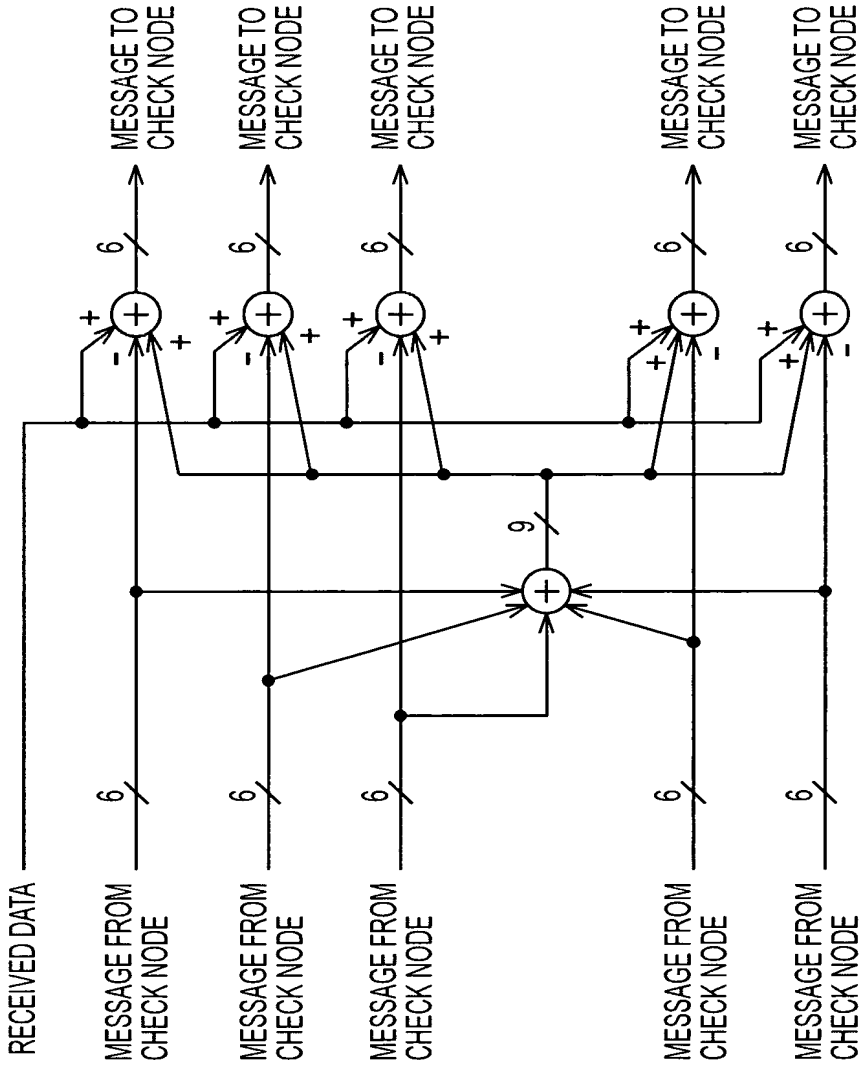

RECEIVED DATA
MESSAGE FROM CHECK NODE
MESSAGE FROM CHECK NODE
MESSAGE FROM CHECK NODE
MESSAGE FROM CHECK NODE
MESSAGE FROM CHECK NODE
MESSAGE TO CHECK NODE
MESSAGE TO CHECK NODE
MESSAGE TO CHECK NODE
MESSAGE TO CHECK NODE
MESSAGE TO CHECK NODE
6
9
+
-

FIG. 15

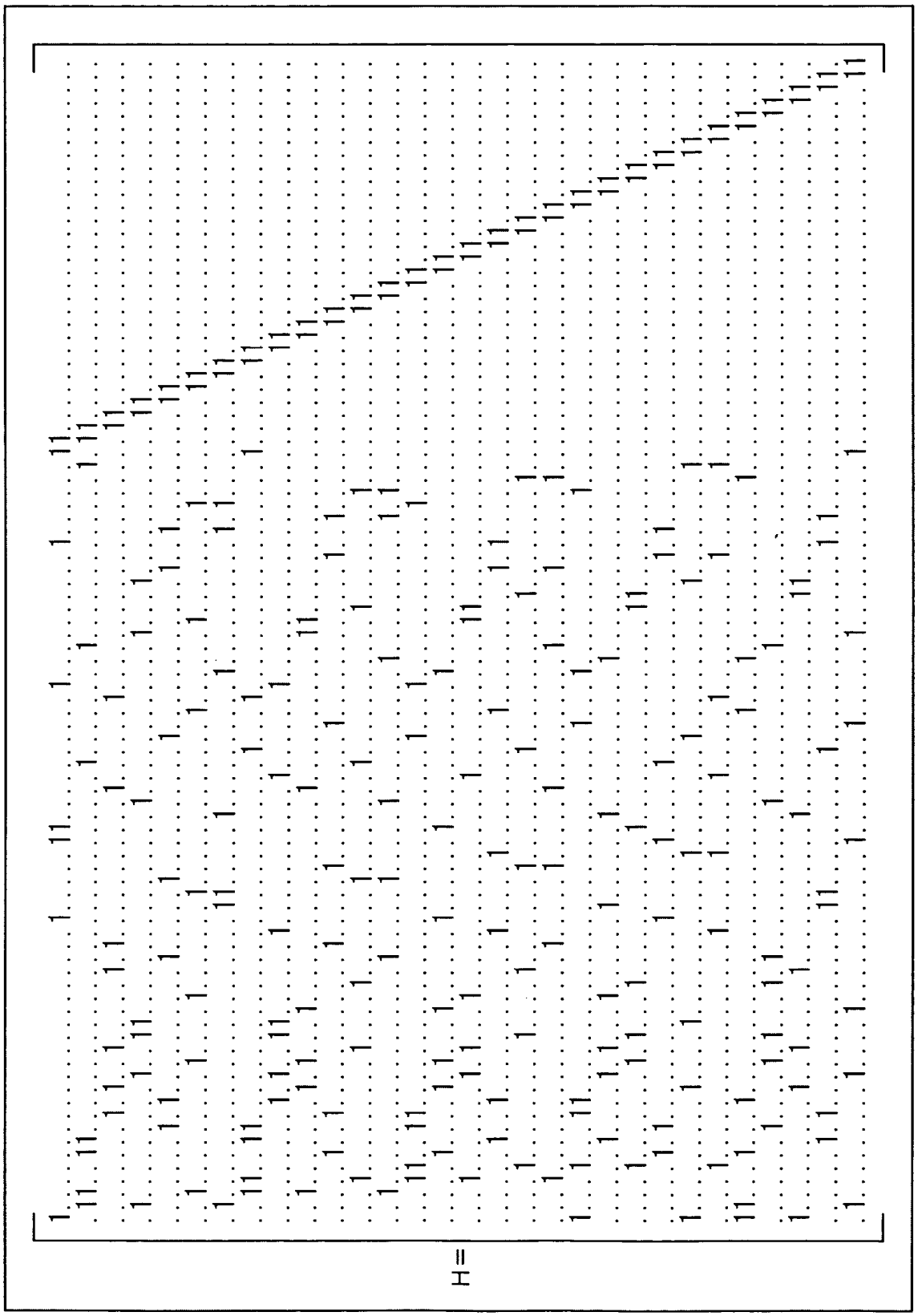


FIG. 16

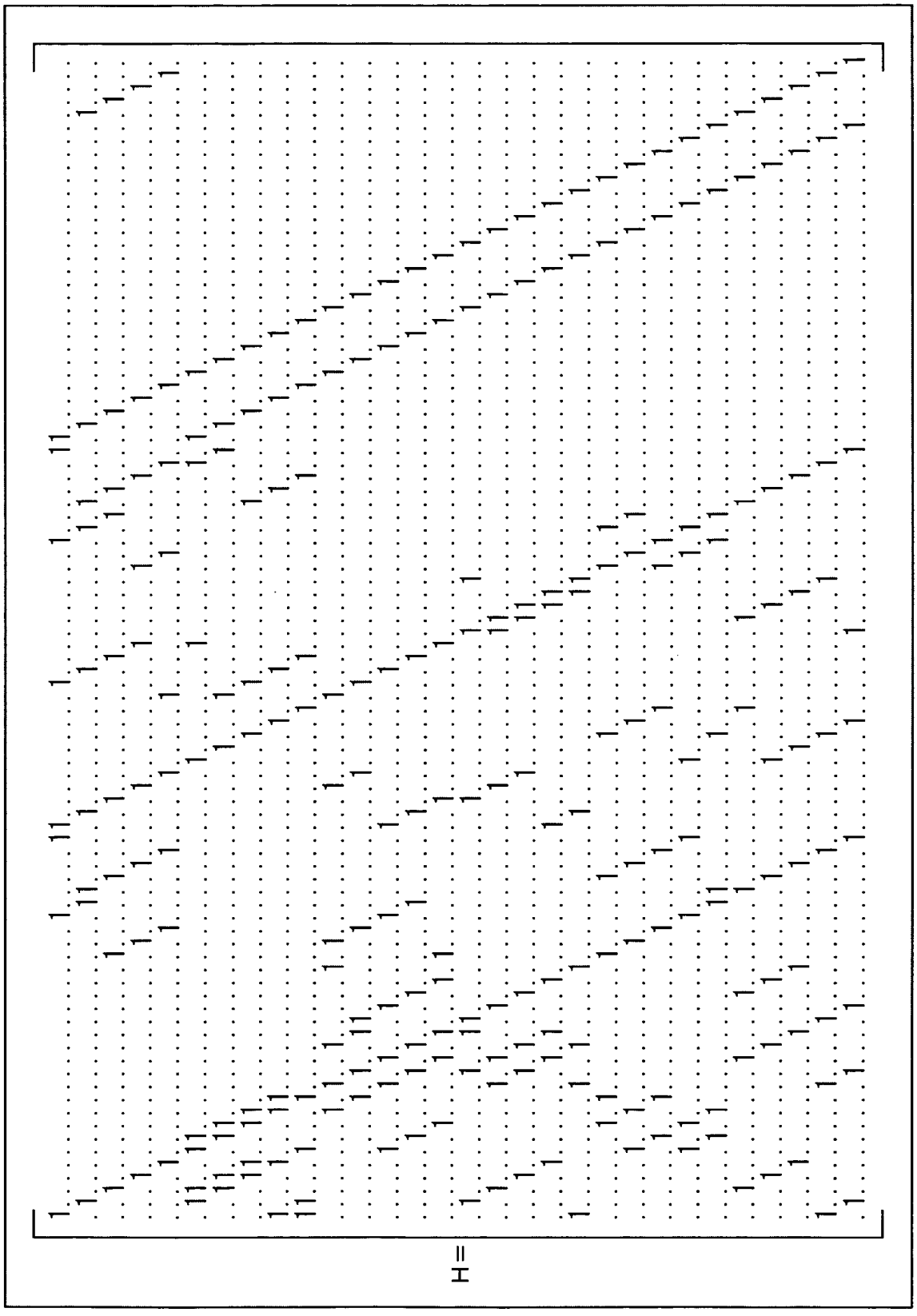


FIG. 17

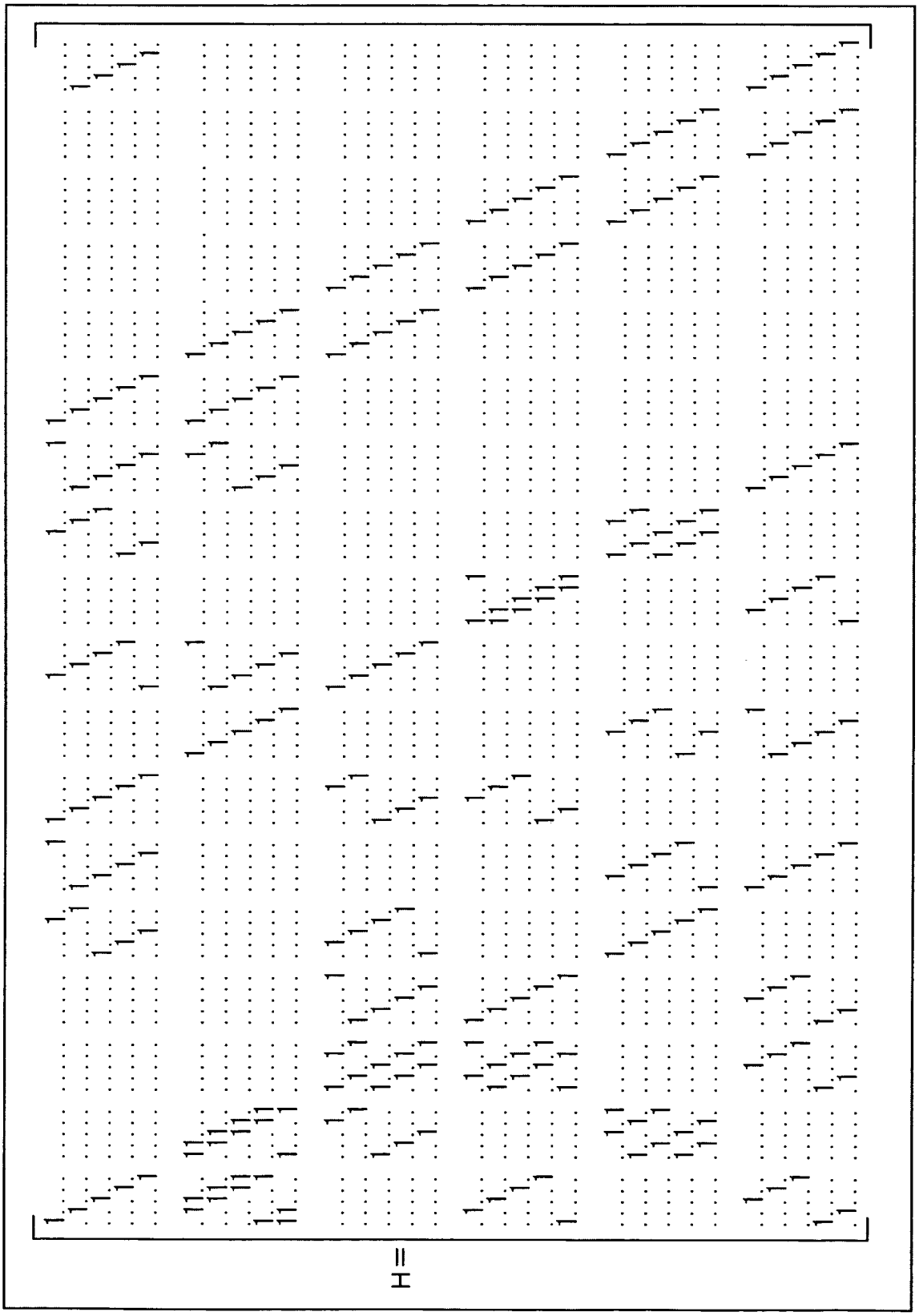


FIG. 18A

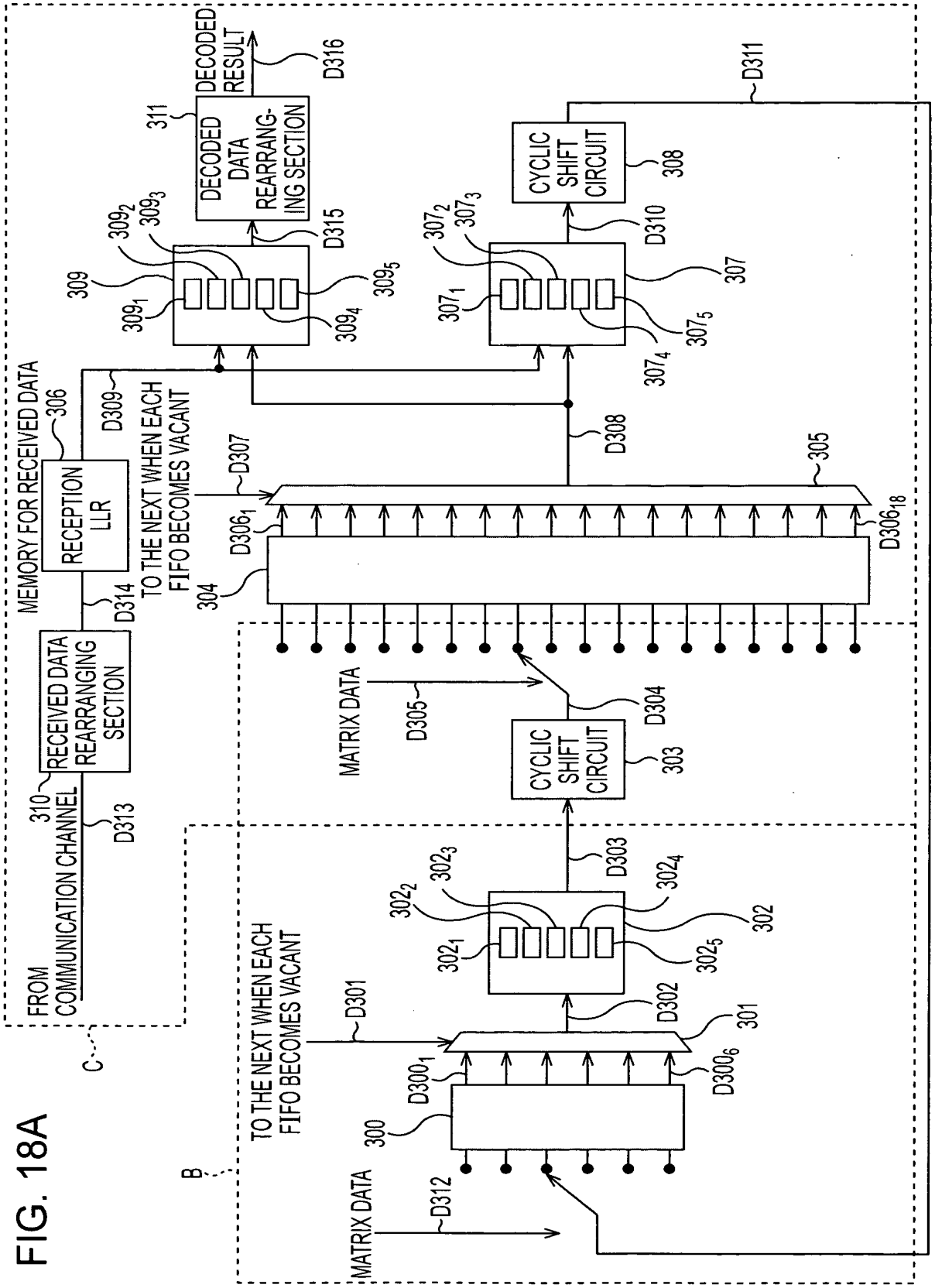

FROM COMMUNICATION CHANNEL
310
D313
RECEIVED DATA REARRANGING SECTION
D314
MEMORY FOR RECEIVED DATA
306
RECEPTION LLR
D309
TO THE NEXT WHEN EACH FIFO BECOMES VACANT
D307
D306$_1$
D306$_{18}$
304
305
MATRIX DATA
D305
D304
CYCLIC SHIFT CIRCUIT
303
D303
302$_1$
302$_2$
302$_3$
302$_4$
302$_5$
302
D302
301
D301
TO THE NEXT WHEN EACH FIFO BECOMES VACANT
D300$_1$
D300$_6$
300
MATRIX DATA
D312
B
C
309
309$_1$
309$_2$
309$_3$
309$_4$
309$_5$
DECODED DATA REARRANGING SECTION
311
DECODED RESULT
D316
D315
307$_1$
307$_2$
307$_3$
307$_4$
307$_5$
307
CYCLIC SHIFT CIRCUIT
308
D310
D311
D308

FIG. 18B

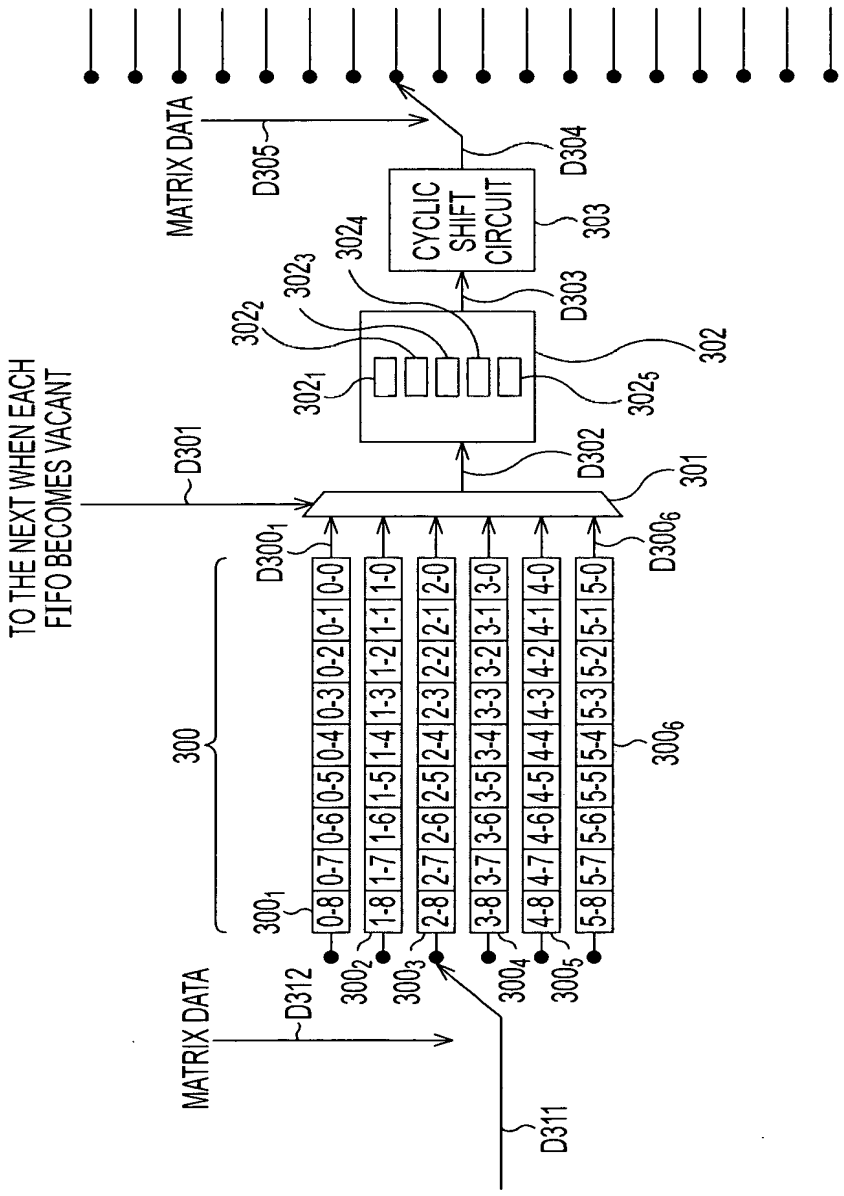

TO THE NEXT WHEN EACH FIFO BECOMES VACANT
MATRIX DATA
D305
D304
CYCLIC SHIFT CIRCUIT
303
3024
3023
3022
3021
D303
302
3025
D301
D302
301
D3001
D3006
300
3001
3006
MATRIX DATA
D312
3002
3003
3004
3005
D311

FIG. 18C

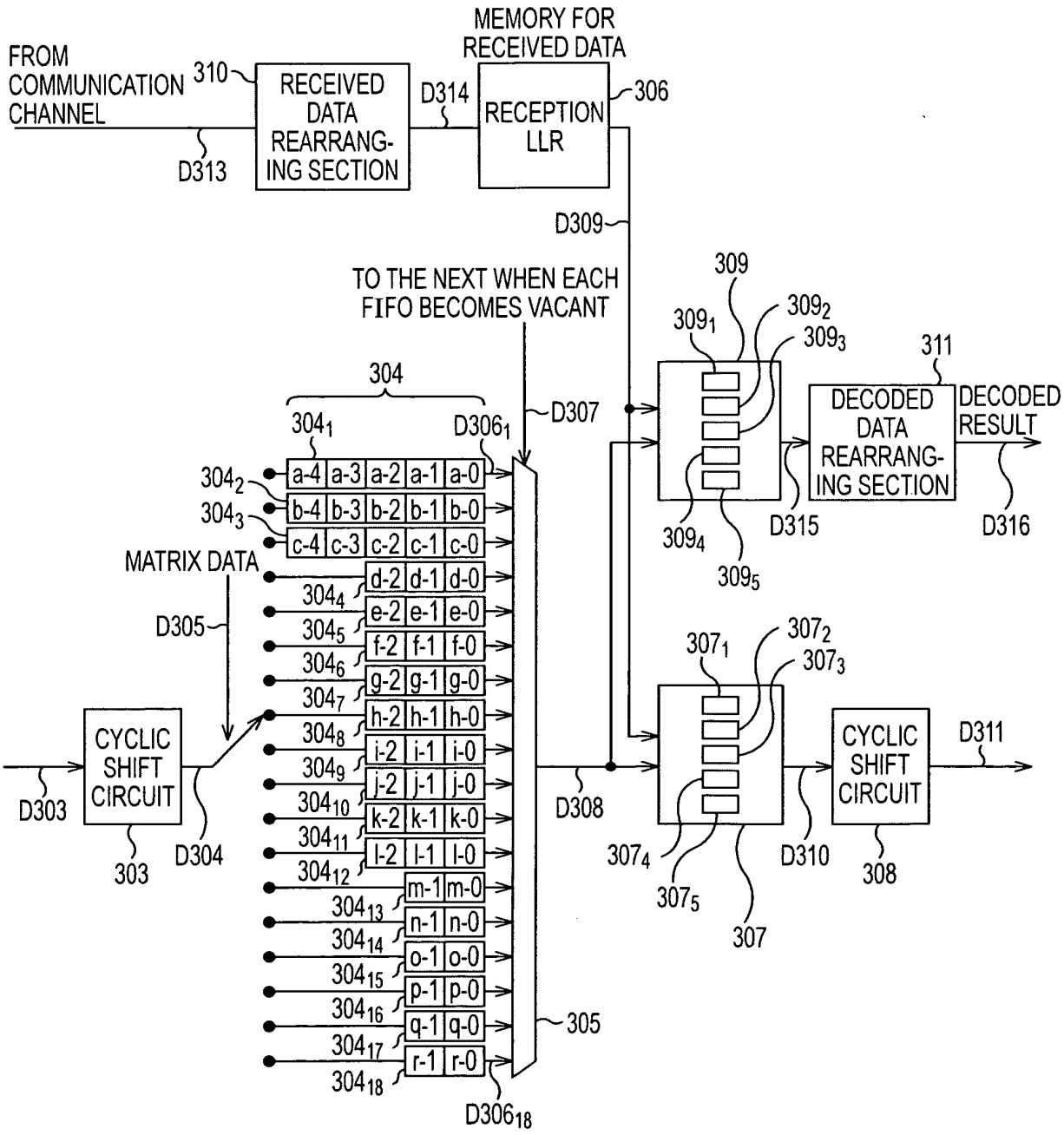
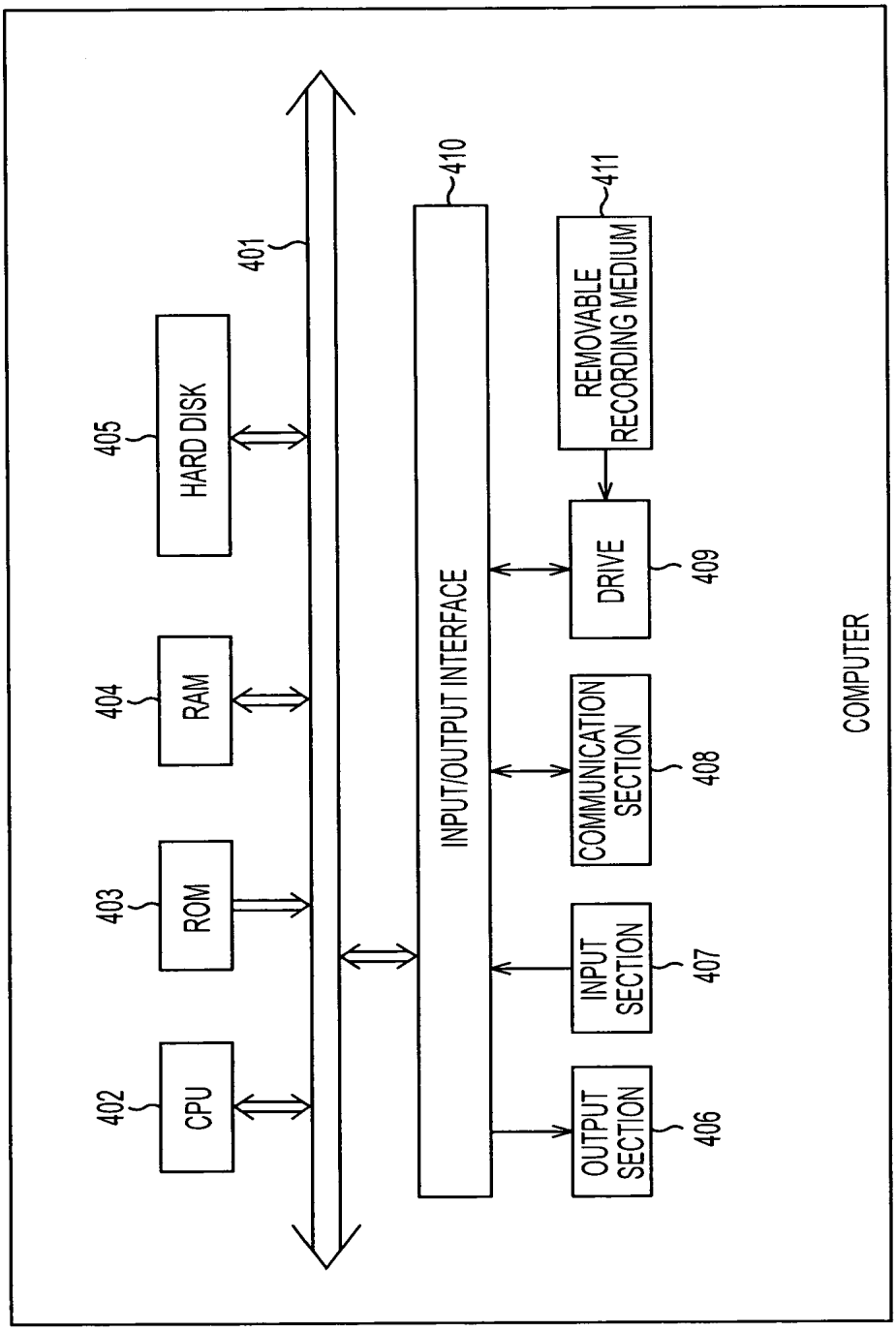

FROM COMMUNICATION CHANNEL
310
RECEIVED DATA REARRANG-ING SECTION
D313
D314
MEMORY FOR RECEIVED DATA
RECEPTION LLR
306
D309
TO THE NEXT WHEN EACH FIFO BECOMES VACANT
309
309$_1$
309$_2$
309$_3$
309$_4$
309$_5$
311
DECODED DATA REARRANG-ING SECTION
DECODED RESULT
D315
D316
304
304$_1$
D306$_1$
D307
304$_2$
304$_3$
a-4 a-3 a-2 a-1 a-0
b-4 b-3 b-2 b-1 b-0
c-4 c-3 c-2 c-1 c-0
MATRIX DATA
D305
304$_4$
304$_5$
304$_6$
304$_7$
304$_8$
304$_9$
304$_{10}$
304$_{11}$
304$_{12}$
304$_{13}$
304$_{14}$
304$_{15}$
304$_{16}$
304$_{17}$
304$_{18}$
d-2 d-1 d-0
e-2 e-1 e-0
f-2 f-1 f-0
g-2 g-1 g-0
h-2 h-1 h-0
i-2 i-1 i-0
j-2 j-1 j-0
k-2 k-1 k-0
l-2 l-1 l-0
m-1 m-0
n-1 n-0
o-1 o-0
p-1 p-0
q-1 q-0
r-1 r-0
305
D306$_{18}$
CYCLIC SHIFT CIRCUIT
D303
303
D304
D308
307$_1$
307$_2$
307$_3$
307$_4$
307$_5$
307
D310
CYCLIC SHIFT CIRCUIT
308
D311

FIG. 19


COMPUTER
CPU
402
ROM
403
RAM
404
HARD DISK
405
401
INPUT/OUTPUT INTERFACE
410
OUTPUT SECTION
406
INPUT SECTION
407
COMMUNICATION SECTION
408
DRIVE
409
REMOVABLE RECORDING MEDIUM
411